PATENT

Attorney Docket No.: 10003522-1
U.S. Patent Application Serial No.: 09/915,510

REMARKS

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. Claims 1-20 and 23-25 are pending, of which claims 1, 23, and 25 are independent.

Claims 1-3, 5, 7-16, 18-20 and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. (6,708,069) in view of Kelly (5,734,872) in further view of admitted prior art. Claim 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kardach et al. (5,560,001).

Claims 15-17 were rejected under 35 U.S.C. § 112 second paragraph. Claim 1 was objected to and claims 1-20 were rejected under 35 U.S.C. § 112 second paragraph as being indefinite. Claims 4 and 6 were objected to as including allowable subject matter but being dependent on a rejected base claim.

The above rejections are respectfully traversed for at least the reasons set forth below.

Claim Objection

Claim 1 was objected to because claim 1 recites "a programmable device" and "a second programmable device", and it is allegedly confusing. As recommended by the Examiner, claim 1 has been amended to recite a first programmable device. Accordingly, the objection to claim 1 has been overcome.

PATENT

Attorney Docket No.: 10003522-1
U.S. Patent Application Serial No.: 09/915,510

Claim Rejection Under 35 U.S.C. §112

Claims 15-17 were rejected claims under 35 U.S.C. § 112 second paragraph as being indefinite. Claims 15-17 have been amended to recite "at least one of the first programmable device and the second programmable device" to avoid any further confusion. Accordingly, the rejection to claims 112 second paragraph rejection of claims 15-17 has been overcome.

Claim Rejection Under 35 U.S.C. §103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

1. Claims 1-3, 5, 7-16, 18-20 and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of Kelly in further view of admitted prior art.

Ohashi et al. discloses a distributed control system including a plurality of nodes, wherein each node includes a processor. See figure 1. Examples of the distributed control system include a semiconductor production system, a home/building automation system, and a medical system.

Ohashi et al. discloses that each of the nodes transmits and receives messages via a transmission line 100. For example, when a node transmits a message, the message is broadcasted on the transmission line 100. Every node connected to the transmission line 100 receives the message and determines whether the message is intended for a respective node by comparing information in the message to information stored in the respective node. A filtering circuit 205 in each node performs the comparison, and thus determines whether a node receiving the message should process the message.

The filtering circuit 205 is shown in detail in figure 3. A message is received and stored in 301. The comparison parts 3031-3033 compare information in the message with information stored in the registration parts 3021-3023. The control part 304 receives the comparison results for each of the comparison parts 3031-3033. If all of the comparison results indicate an "agreement" then the message is stored in 305 and eventually processed by the CPU 201 of the node. If any of the comparison parts outputs a result of "disagreement", the message is abandoned from the storing part 301. See column 9, lines 34-47.

Claim 1 recites,

> a bus processing block coupled to the bus interface circuit, the bus processing block implemented with a first programmable device and configured to perform selected processing in response to selected bus messages; and
>
> a filter circuit coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a second programmable

device and configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block.

The rejection of claim 1 states that the claimed bus processing block with a programmable device is taught by the control part 304 shown in figure 3 of Ohashi et al., and the claimed bus interface circuit is taught by structure 205, *i.e.*, the filtering circuit 205, shown in figure 3 of Ohashi et al.

Firstly, Ohashi et al. fails to teach or suggest a bus processing block implemented with a first programmable device. Ohashi et al. does not disclose the control part 304 is programmable. If this rejection is maintained, the Examiner must indicate where Ohashi et al. discloses that the control part 304 is programmable.

Secondly, Ohashi et al. fails to teach or suggest a filter circuit configured to direct bus messages to a selected one of the bus interface and the bus processing block. According to an embodiment of the Applicant's invention, the filter circuits 204 or 206 shown in figure 2 select either the bus processing block 208 or the bus interface 202 for processing a message. In one example, messages needing customized processing, which is implemented through the programmable processing block 208 programmed to provide the customized processing, are directed to the processing block 208. Messages not needing the customized processing are directed to the bus interface. Thus, the filters 204 and 206 perform a selection process, which ensures the processing block 208 is not burdened with operations for which customized processing is not desired.

Ohashi et al., on the other hand, fails to teach or suggest a filter circuit configured to direct bus messages to a selected one of the bus interface and the bus processing block. Instead, all the messages transmitted on the transmission line 100 shown in figure 3 of Ohashi

et al. are taken in by the filtering circuit 205 of Ohashi et al. The filtering circuit 205 either stores a message 310 in the storing part 305 or does not store the message 310 in the storing part 305 based on a comparison of message identifying portions of the message 310 with stored identifying portions stored in the registration parts. As discloses in Ohashi et al., the comparison parts 3031-3033 compare information in the message with information stored in the registration parts 3021-3023. The control part 304 receives the comparison results for each of the comparison parts 3031-3033. If all of the comparison results indicate an "agreement" then the message is stored in 305 and eventually processed by the CPU 201 of the node. If any of the comparison parts outputs a result of "disagreement", the message is abandoned from the storing part 301.

The rejection of claim 1 states that column 7, last line through column 8, lines 1-4 of Ohashi et al. discloses comparing the message-sending condition-identifying portions and a message either goes through or by-passes the control parts 304. On the contrary, Ohashi et al. discloses that the control part 304 always determines whether to store a message in the storing part 305. Thus, the control part 304 is never bypassed. Hence, Ohashi et al. fails to teach or suggest selecting one of a bus interface and a bus processing block for directing a message thereto.

The rejection states that Ohashi does not explicitly disclose the filter circuit is implemented with a programmable device but it would have been obvious to use the FPGA of Kelly for the filter circuit 205 of Ohashi because Kelly teaches one to improve performance by employing an FPGA to perform any pre-processing for the CPU.

It would not have been obvious to one of ordinary skill in the art to use an FPGA for the filtering circuit 205 of Ohashi et al. because there is no reason to make the filtering circuit

205 programmable and it would unduly increase the cost and complexity of the device of Ohashi et al. The filtering circuit 205 of Ohashi et al. performs a function of comparing identifying portions of a message to stored identifying portions to determine whether a node receiving the message was an intended destination for the message. Unlike, the bus processing block 208 of an embodiment of the Applicant's invention, which may be customizable to perform operations that are implementation specific to a particular system, the filtering circuit 205 always performs the same function, i.e., a simple comparison, regardless of the implementation, such as regardless of what type of node in Ohashi et al. is using the filtering circuit 205. Thus, there is no need to make the filtering circuit 205 programmable and it would not have been obvious to make the filtering circuit 205 programmable. Furthermore, the motivation is improper. Making the filtering circuit 205 of Ohashi et al. programmable does not improve the performance of the node, as stated in the rejection, because an FPGA performing the function of the filtering circuit 205 results in the same comparison being performed but using a different circuit. Accordingly, claims 1-3, 5, 7-16, 18-20 are believed to be allowable.

Independent method claim 23 recites,

> selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit.

Ohashi et al. fails to teach or suggest this feature. The rejection of claim 23 states that the control part 304 of Ohashi et al. performs selected processing in response to selected bus messages.

As described above, all the messages taken in from the transmission line 100 shown in figure 3 of Ohashi et al. are processed by the filtering circuit 205 including the control part 304. See column 7, lines 62-63. Thus, the filtering circuit 205 of Ohashi et al., which the rejection alleges to include the claimed bus processing block and the claimed bus interface circuit, processes all the messages rather than selecting classes of messages to process by either the bus processing block or the bus interface circuit.

Independent claim 25 recites a similar feature, which includes,

> means for selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit.

The claimed selecting recited in claim 23 and the claimed means for selecting recited in claim 25 are not taught or suggested by either Ohashi et al. or the admitted prior art. Thus, claims 23-25 are also believed to be allowable.

2. Claims 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kardach et al.

Claims 17 is believed to be allowable for at least the reasons claim 1 is believed to be allowable. In addition, it would not have been obvious to combine the microcode engine of Kardach et al. with Ohashi et al. in view of the admitted prior art.

Claims 17 recites the programmable device [of the bus processing block] includes a microcode engine. The rejection substitutes the logic of the processing block of Ohashi et al., which as stated in the rejection is the control part 304, with the microcode engine of Kardach et al. The stated motivation for this modification and combination is that it would improve

performance by employing a microcode engine to perform any pre-processing for the CPU. However, simply substituting a microcode engine for another type of logic does not improve performance. Thus, the motivation is improper. In addition, there is no need to make the control part 304 of Ohashi et al. programmable. The control part 304 simply determines whether the comparison results are all in agreement. This function remains the same regardless of the type of message or the processing to be performed on the message by the CPU. Thus, there is no need to make the control part 304 programmable. In fact in may be prohibitive to do so, because of increased costs resulting from using programmable logic, such as a microcode engine, instead of cheaper logic.

Furthermore, Ohashi et al. and Kardach et al. are unrelated. Kardach et al. is directed to a method of operating a processor at reduced speed. Ohashi et al. is directed to handling broadcasted messages in a distributed control system, such as a semiconductor production system, a home/building automation system, and a medical system, which is unrelated to controlling processor speed. Thus, it would not have been obvious to one of ordinary skill in the art to combine Kardach et al. with Ohashi et al.

PATENT

Attorney Docket No.: 10003522-1
U.S. Patent Application Serial No.: 09/915,510

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Boon Seong Ang

Dated: March 21, 2005 By _____
Ashok K. Mannava
Registration No.: 45,301

MANNAVA & KANG, P.C.
8221 Old Courthouse Road
Suite 104
Vienna, VA 22182
(703) 652-3822
(703) 880-5270 (facsimile)